Low-voltage, low-power, low switching error, class-AB switched current memory cell

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A class-AB switched current memory cell is proposed. The circuit decomposes the input signal into two components by a low-voltage class-AB current splitter and subsequently processes the individual signals by two low switching error class-A memory cells. As a consequence, the output current obtained by recombination of the separated signals can be higher than the bias current and features low error. Simulation results confirm that, for a 0.75 V supply, a 5 MS/s sampling frequency, and a 500 kHz sinusoidal input current having 400% modulation index, the proposed memory provides less than −45 dB THD output current with very low switching error.

Introduction: To gain signal dynamic range and power efficiency of analogue sampled data signal processing in standard digital CMOS processes, class-AB switched current (SI) memory cells also known as current track and hold (CTH) circuits, which are the basic cells of analogue sampled data signal processors, have been developed over the years. Most of the class-AB SI memory circuits are based on complementary devices connected in anti-series in a stacked topology [1–4]. Therefore, these SI circuits cannot operate from a very low supply voltage (VDD) and, for the circuits of [2–4], require an additional circuit controlling their quiescent currents. Furthermore, the switching error induced by clock feedthrough and charge injection effects leads to the requirement of a cancellation circuit and/or a complicated clock scheme.

In this Letter, we propose a class-AB SI memory cell without the stacked connection, the requirement of a quiescent current control circuit or a complicated clock scheme. The stacked connection and the current control circuit can be circumvented by using a signal splitting approach that decomposes the input signal into two components that can be separately processed by class-A cells formed by identical devices. In fact, the signal splitting approach has already been used in [1]; however, here it requires a stacked connection and different types of class-A cells (pMOS and nMOS, respectively), which does not allow for low-voltage operation. It has been shown in [5] that, by inserting a voltage follower/level shifter (VF) and a switch into the class-A memory cell, more than 90% of the switching error can be removed. We thus apply the technique of [5] to the proposed circuit as well to improve the performance further. For 0.13 μm CMOS IC process technology, the proposed circuit can operate in class-AB from very low supply voltage, consumes very low quiescent power and almost completely rejects the switching error.

Fig. 1 Class-AB switched current memory block diagram

Class-AB block diagram: Fig. 1 shows the block diagram of the proposed class-AB memory cell comprising a current splitter, identical class-A CTH circuits (THA and THB) and a current combiner. The current splitter functions as an input stage that splits the input current Iin into two components (I1 and I2) under the condition that

\[ I_{in} = I_1 - I_2 \]  

Signals I1 and I2 are injected to THA and THB, respectively, in order to be separately tracked and held before combining again at the output according to

\[ I_{out} = I_{11} - I_{22} \]

Hence, the recombined output signal Iout corresponds to the input signal Iin which has been tracked and held.

Circuit description: The current splitting input stage is constituted by a low-voltage class-AB transconductor [6] connected in closed-loop configuration as shown Fig. 2a. All current mirror circuits (M4–M6, M11–M12, M13–M14) provide unity gain. Transistor sizes of M3–M8 are identical and M1 and M2 are also equally sized. Reference voltage Vref supply voltage VDD and bias current Iref are set for biasing all transistors in strong inversion saturation. By employing negative feedback, Iref can be injected at the drain terminals of M6 and M8 where it is split into the drain currents of M1 (I1) and M6 (I2), the latter equals the drain current of M8. The split currents I1 and I2 are subsequently copied again by transistors M4 and M7, respectively, and finally the direction of them is inverted to interface with the subsequent stages by current mirrors M11–M12 and M13–M14. Note that owing to the square law behaviour of MOSFETs in strong inversion saturation, for this circuit (1) is valid in the range of Iin ≥ 4 Iref [6], allowing the circuit to process input currents with a modulation index up to four.

Fig. 2 Proposed class-AB switched current memory cell

a Current splitter
b Class-A memory cells with switching error reduction

Fig. 2b shows the identical class-A CTH circuits THA (M1A, M2A, and switch M1A) and THB (M1B, M2B, and switch M1B) with the VF formed by a flipped voltage follower circuit (M1C–M2C and Io) [6] and switch M5C, which is connected to Vref. The VF and switch M5C are inserted to reduce the switching error induced by the sampling switches of both THA and THB circuits (M3A and M3B) [5]. The incoming signals of the CTH circuits are supplied by the current splitter and its sampling and holding phases are controlled by clock signal Vclk, which has a swing close to VDD. At the end of the sampling phase (all switches are turned off), a voltage switching error or feedthrough error (Vcft) will appear at the gate of the M2B. Since the gate-source voltage of M2C is nearly constant (regulated by Io) [6], the Vcft at the gate terminal of M2C will relax onto the common source node of the memory transistors (M2A and M2B), effectively cancelling the switching error. As a consequence, the current error at the hold phase is eliminated. The recombined output current defined by (2) can be simply achieved by inserting a unity gain current mirror into the output lead of either THA or THB and adding its output current to the output current of THB or THA.

Simulation results: The class-AB SI memory cell in Fig. 2 was simulated in Cadence using RF Spectre and 0.13 μm CMOS model parameters. Transistor widths (W) and lengths (L) are defined in Table 1. To minimise the charge injection and clock-feedthrough effects, the dimensions of the sampling switches were set to be as
small as the process allows. To minimise switching error, the compensa-
tion switch was sized to be double of the dimension of the sampling
switches. \( V_{DD} = 0.75 \text{ V}, \ V_{ref} = 0.3 \text{ V}, \) and \( I_o = 1 \mu\text{A}. \) The quiescent
power equals 8.25 \( \mu\text{W}. \)

Table 1: Transistor dimensions

<table>
<thead>
<tr>
<th>Transistor</th>
<th>( W (\mu\text{m}) )</th>
<th>( L (\mu\text{m}) )</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 – M2, M3 – M8, M1A – M2A, M1B – M2B, M2C</td>
<td>5</td>
<td>0.5</td>
</tr>
<tr>
<td>M1C</td>
<td>3</td>
<td>0.3</td>
</tr>
<tr>
<td>M3A – M5B</td>
<td>0.15</td>
<td>0.13</td>
</tr>
<tr>
<td>M7C</td>
<td>0.15</td>
<td>0.26</td>
</tr>
<tr>
<td>M9 – M14</td>
<td>10</td>
<td>1</td>
</tr>
</tbody>
</table>

Transient responses of the memory cell employed as a CTH circuit for
a 4 \( \mu\text{A}, \) 500 kHz sinusoidal input current (modulation index = 4) and
5MS/s sampling rate are demonstrated in Figs. 3 and 4. In Fig. 3, the
solid and dashed lines represent \( I_{o1} \) and \( I_{o2}, \) respectively. The waveforms
are obtained by nonlinear splitting at the input stage and tracked and held
by the class-A THA and THB, respectively, for \( I_{o1} \) and \( I_{o2}. \) In Fig. 4,
compared to the input current represented by the grey line, we can see
that after combining, the output current, represented by the black line,
becomes a sinusoidal waveform again. Using discrete-time Fourier
transform analysis, the output waveform shows less than –45 dB total
harmonic distortion.

Fig. 3 Transient responses of sampled splitting currents in class-AB
switched current memory cell

--- \( I_{o1} \)

--- \( I_{o2} \)

Fig. 4 Transient responses of output and input currents in class-AB switched
current memory cell

--- input current

--- output current

Conclusion: A new class-AB switched current memory cell employing
current splitting is presented. By using a low-voltage class-AB current
splitter circuit, the input signal can be separated into two unipolar cur-
rents to be processed further by two low switching error class-A
memory cells. Thanks to the class-AB operation and switching error
rejection, the input signal of the proposed circuit can be raised up to
time four times higher than the bias current, and produces a very clean
output current waveform (low glitch, low error) and relatively low
distortion.

© The Institution of Engineering and Technology 2008
11 April 2008
Electronics Letters online no: 20081030
doi: 10.1049/el:20081030
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