Biphasic Stimulator Circuit for a Wide Range of Electrode-Tissue Impedance Dedicated to Cochlear Implants

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Abstract—This paper presents an implementation of a least voltage drop neural biphasic stimulator circuit applied in cochlear implants. Using a double loop negative feedback topology, the output impedance of the current generator is increased, while requiring only one effective drain-source voltage drop (\(V_{\text{eff}}\)). This allows the circuit to convey more charge into the tissue. The circuit can provide a biphasic stimulation scheme from a single ended supply with an amplitude range of 10\(\mu\)A up to 1.05mA for a wide range of electrode-tissue impedances, \(R_L=1k\Omega\sim10k\Omega, C_L=1nF\sim10nF\). The stimulation current is set by scaling a reference current using a two stage binary-weighted transistor DAC configuration (3 bits HV transistor DAC and 4 bits LV transistor DAC) to improve the speed of stimulation pulses and minimize the area of the circuit. Simulation results, using the AMS 0.18\(\mu\)m high-voltage CMOS process, show that the charge error within a cycle (600\(\mu\)s) is only 0.02\%, equivalent to a DC current error of 3nA at the maximum stimulation current with a load of 10k\(\Omega\)+10nF.

I. INTRODUCTION

Implantable neural stimulators, such as cochlear implants [1] and deep brain stimulators [2] are becoming an important treatment method for a wide variety of pathologies [3]. The design of such implants imposes strict requirements on safety, power consumption and size.

Because the stimulators are implanted inside the body, the device must be as small as possible. This means avoiding the use of external components, while simultaneously keeping the power consumption as low as possible to avoid the need for big batteries. Therefore the voltage compliance of the circuit must be as high as possible to allow for the lowest supply voltage possible.

In case of constant current-mode stimulation, the output impedance of the current source needs to be high to guarantee a well defined output current for a wide range of loads. This is particularly important for charge cancellation purposes.

This paper discusses the implementation of a constant current mode, biphasic neural stimulator for cochlear implants which meets the demands mentioned above. In section II the system design is discussed, Section III gives an overview of the implementation at circuit level, while section IV shows the simulation results.

II. CONCEPT OF THE STIMULATOR CIRCUIT

This design employs a biphasic constant current-mode stimulation scheme, which is depicted in Fig. 1c. By employing a constant current \(I_{\text{stim}}\) for a particular time \(t_c, (t_a)\) the charge \(Q = I_{\text{stim}} t_c = -I_{\text{stim}} t_a\) is controlled, which makes charge cancellation possible for safety reasons.

It was chosen to use a single power supply to avoid the need for two accurate matched stimulation current sources [4]. For a single ended implementation a switch array is needed to reverse the direction of the current as depicted in Fig. 1a. Switch \(S_1\) is used for the positive current pulse and \(S_2\) for the negative current pulse. Switch \(S_1\) is used after switch \(S_2\) to discharge the tissue passively to allow the residual charge to be removed.

The electrode-tissue model is represented by \(Z_L\): a series \(RC\) circuit as shown in Fig. 1b. It is assumed in the design that the values for the components can be in the range \(R_L=1k\Omega\sim10k\Omega, C_L=1nF\sim10nF\). The currents used for stimulation are in the range of \(I_{\text{stim}}=10\mu\text{A}\sim1\text{mA}\).
The implementation of the current source in Fig. 2 is based on the double loop negative feedback topology as proposed in [5]. The first internal feedback loop (comprising amplifier $A_v$ and M3) is used for high precision scaling with a factor $m$ of the stimulation current $I_{stim}$ by making the drain voltages of M1 and M2 equal. This realizes the high output impedance of the current source without sacrificing voltage headroom ($V_{in}$ is only one effective $V_{ds}$ of M2). The second feedback loop (comprising amplifier $Z_m$) accurately sets $I_r$ (and thereby $I_{stim}$) equal to $nI_{ref}$ by forcing the error current $I_e = 0$. The two feedback loops described above now give the relationship:

$$I_{stim} = m \cdot n \cdot I_{ref}. \tag{1}$$

It is possible to adjust $I_{stim}$ by controlling the factors $m$ and $n$. Both current mirrors are implemented using a binary weighted DAC scheme, to be discussed in the next section.

III. CIRCUIT IMPLEMENTATION

The implemented stimulator circuit is shown in Fig. 3. A high voltage supply (≥10V) is needed to accommodate the maximum current through the maximum load. This requires the use of high-voltage (HV) transistors (indicated by the thick drain terminal) combined with low-voltage (LV) transistors. To minimize the area occupied by the circuit, the number of HV transistors applied should be as small as possible.

A. High-voltage and Low-voltage DAC configuration

In Fig. 3 the implementation of the two DACs is shown in the blue shaded area. In order to achieve a 10μA resolution for a 1mA full scale stimulation current, a resolution of 7 bits is required.

The number of bits in the HV DAC should be chosen as small as possible. This will reduce the number of (large) HV transistors resulting in a smaller area as well as a lower parasitic capacitance. However, a certain minimum equivalent transistor size is needed to be able to supply the maximum stimulation current. Simulations have shown that a minimum of 3 bits is needed for the HV DAC.

The remaining 4 bits can be implemented using LV transistors. These transistors are much smaller, making the area contribution negligible compared to the HV DAC.

The reference current chosen is $I_{ref} = 10\mu A$. By enabling one or more transistors in the binary weighted DACs (using the switches), $I_{stim}$ can be made programmable using the following relation:

$$I_{stim} = \left(\sum_{k=0}^{u-1} 2^k\right) \left(\sum_{l=0}^{l-1} 2^l\right) I_{ref}, \tag{2}$$

in which $u$ and $l$ are the bit-numbers of the enabled HV transistors M2 and LV transistors M7, respectively. In this way the LV DAC can generate a current in steps of 10μA from 10μA to 150μA. The HV DAC can scale this current with a factor 1 up to 7, resulting in a maximum stimulation current of 1.05mA.

B. Switch array

The design of the switch array is not trivial, due to the large range of voltage potentials at the tissue. Because of the charging of $C_L$ and the subsequent reversing, the potential can be negative. Furthermore the swing can go up to almost $V_{DD}$.

The negative potentials make NMOS transistors at the ground terminal less suitable, because of the parasitic diode between the drain and the substrate (biased at 0V). This diode will be conducting when the drain potential will be <0V. This can be solved by placing an isolated Shottkey diode in series as depicted in Fig. 4. This diode will have a small 0.4V voltage drop, which leads to only a minor loss of voltage headroom.

The upper switches can be implemented using simple PMOS HV transistors, because those are isolated from the substrate using a deep N-well.

Switch $S_3$ is implemented using back to back PMOS transistors with the source terminals biased at 18V. The back to back configuration is necessary because of the parasitic diode between drain and source: in this way one of the diodes is always reverse biased, preventing leakage.

The upper switches can be implemented using simple PMOS HV transistors, because those are isolated from the substrate using a deep N-well.
Finally a standard cross coupled level shifter is used to convert a LV control signal to a HV signal for $V_{control}$.

C. Differential Amplifier $A_v$

Amplifier $A_v$ is used in the feedback loop to control $V_d$ of M1. It is implemented using a standard differential amplifier (using HV transistors) with an active load as depicted in Fig. 5.

An offset voltage source is needed at the output of the amplifier to bias the gate of M3 properly. The floating voltage source was introduced using a diode connected LV transistor chain and current sources $I_B = 5\mu A$. The minimum common mode input voltage the amplifier can handle is about 3V because of the biasing of the LV DAC. When $V_d < 3V$ an error is introduced in the output current because $V_{DS,M2} > V_{DS,M1}$. However this error is small because $V_{DS,M2} >> V_{DS,M1} - V_{DS,M2}$.

IV. SIMULATION RESULT

To verify the performance of the stimulator circuit the 0.18\mu m AMS HV process technology was used for simulations on the implemented circuit shown in Fig. 3. The supply voltage was set at 18V in order to have enough voltage headroom (1.05mA through $R_L=10k\Omega$, while $C_L=10nF$ is charging). The dimensions of the transistors are indicated in Table 1.

To check the functionality of the circuit, a few stimulation cycles are simulated for a variety of tissue impedances and stimulation parameters.

Fig. 6 shows a stimulation cycle with $t_d = t_i = t_c = 50\mu s$ and a total cycle time of 600\mu s as can be seen from the control signals for $S_1$, $S_2$ and $S_3$. The electrode potential $V_{stim}$ is plotted for $I_{stim} = 500\mu A$ with a load of $10k\Omega + 10nF$. As can be seen the voltage first jumps to 5V and then $C_L$ is charged up to about 8V. The figure also shows the charge that is injected into the tissue by the 500\mu A source. The charge goes back to almost 0 C after a stimulation cycle, assuring charge cancellation. The residual charge error will be discussed at the end of this section.

In order to show that the circuit is working properly, the circuit is simulated over the complete range of stimulation currents and tissue impedances.

In Fig. 7 the stimulation current and charge are depicted for the minimum setting $I_{stim} = 10\mu A$, both for the maximum load as well as for the minimum load. In Fig. 8 the same is shown for $I_{stim} = 1.05mA$, the maximum stimulation current. In the last case the pulse widths $t_d$ and $t_i$ were reduced to 10\mu s to prevent the tissue from clipping to the supply voltage. As can be seen from both figures the circuit is working as expected and charge cancellation is achieved. The spikes due to switching that are especially visible for low $I_{stim}$ do not contribute to any significant charge mismatch.

In Fig. 9 the operation of the diode in series with the NMOS switch (Fig. 4) is shown for $I_{stim} = 10\mu A$. It can be seen that during phase $S_1$ the potential at node $n$ becomes negative. However, the reverse biased condition of the diode will keep the voltage at node $d$ positive, preventing leakage.

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>W [\mu m]</th>
<th>$L$ [\mu m]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_1$, $M_2$</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>$M_6$, and $M_7$</td>
<td>0.5</td>
<td>0.18</td>
</tr>
<tr>
<td>$M_3$</td>
<td>5</td>
<td>0.6</td>
</tr>
<tr>
<td>$M_{11}$</td>
<td>10</td>
<td>0.6</td>
</tr>
</tbody>
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TABLE 1. TRANSISTOR DIMENSIONS

Figure 6. Transient simulation waveform of a stimulation current of 500\mu A with a load of $10k\Omega + 10nF$: (a) Switch control signal $S_1$, (b) Switch control signal $S_2$, (c) Switch control signal $S_3$, (d) stimulation current, (e) electrode potential and (f) total charge at the load.
The residual charge at the end of phase \( S_2 \) is very small. For example Fig. 6 (f) shows in the zoomed in part that \( Q = -87 \) pC. By using \( S_1 \) the residual charge is reduced to \(-7.4 \) pC in 450\( \mu \)s. Table 2 shows the percentages of the charge error and the residual DC current error for several values of \( I_{\text{stim}} \). For \( I_{\text{stim}} = 1.05 \) mA the pulse widths \( t_i \) and \( t_d \) were chosen to be 10\( \mu \)s to prevent clipping of \( I_{\text{stim}} \). The relative charge error is calculated by the ratio of the maximum charge injected into the load compared with the residual charge at the end of the cycle. The DC current error is determined by dividing the residual charge by the stimulation period. The results show the charge error and residual DC current error are well below the safety limits mentioned in [4].

<table>
<thead>
<tr>
<th>Stimulation current ((I_{\text{stim}}))</th>
<th>Charge error (%)</th>
<th>DC current error (A)</th>
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<tbody>
<tr>
<td>10( \mu )A (50( \mu )s)</td>
<td>0.006</td>
<td>0.2n</td>
</tr>
<tr>
<td>500( \mu )A (50( \mu )s)</td>
<td>0.03</td>
<td>12n</td>
</tr>
<tr>
<td>1.05mA (10( \mu )s)</td>
<td>0.02</td>
<td>3n</td>
</tr>
</tbody>
</table>

**Figure 7.** Transient simulation waveforms for \( I_{\text{stim}} = 10 \) mA, \( t_i = t_d = 50 \) \( \mu \)s with (a), (b) maximum load and (c), (d) minimum load.

**Figure 8.** Transient simulation waveforms for \( I_{\text{stim}} = 1.05 \) mA, \( t_i = t_d = 10 \) \( \mu \)s with (a), (b) maximum load and (c), (d) minimum load.

Power consumption is dominated by the bias sources in the differential amplifier (30\( \mu \)A) and the current through the DACs, depending on the number of bits enabled in the LV DAC (ranging from 40–158\( \mu \)A). The static current is limited by the biasing of M3. Note that all these bias sources can be switched off when stimulation is not active, yielding no static power consumption. For maximum \( I_{\text{stim}} = 1.05 \) mA through the maximum load (\( R_L = 10 \) k\( \Omega \)) the power efficiency during stimulation is found to be 48%.

**V. CONCLUSIONS**

This paper has presented the implementation of a constant current-mode biphasic stimulator circuit for a cochlear implant using a single power supply. A double loop negative feedback topology was employed to increase the output impedance without sacrificing voltage headroom. The circuit can deliver stimulation amplitudes in the range of 10\( \mu \)A–1.05 mA for a wide range of electrode-tissue impedances: \( R_L = 1 \) k\( \Omega \)–10 k\( \Omega \), \( C_L = 1 \) nF–10 nF. The charge mismatch was found to be well below the safety limits.

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**REFERENCES**


