In wireless receivers, large dynamic range (DR) input signals necessitate additional power consumption in baseband active filters. A 5th order Chebyshev, ladder type, companding SC low-pass filter is described in this paper which provides gain switching based on the instantaneous value of the signal to handle peak-to-average-power ratio (PAPR), thereby reducing power dissipation for a given DR. Companding compresses the high DR input signal, processes it in a lower DR system (the filter in our case) and then expands the signal at the output [1]. Companding is an alternative to AGC, which sets the filter internal gains during the preamble/midamble so that the signal level in the filter is optimal to provide the minimum SNDR required by the specifications. The IEEE 802.11a/g WLAN receiver [2] presents 2 limitations to the use of AGC. First, the standard puts a stringent AGC settling time requirement (<5.8µs). Since the filter needs extra settling time, AGC is implemented after the filter and before the ADC in the receiver baseband. Secondly, the high PAPR of OFDM signals requires headroom of at least 12dB in the DR of the filter. While dynamic impedance and gain scaling techniques have been proposed in the past as an alternative to AGC [3], this work addresses the PAPR problem.

Figure 4.10.1 shows an example of a companding SC discrete integrator [4]. The two non-overlapping clock phases are φ1 (sampling/hold phase) and φ2 (integration phase). S1, S2, S3, S4, Inc and Dec are digital signals. Based on the OTA's output at the end of φ2, S1 and S2 change the input sampling capacitance C1 to switch the integrator gain by a factor of 2 in the next φ2 (compression). S1 and S2 change the output sampling capacitance C2 to provide an inverse gain for the subsequent stage (expansion). The charge (memory) on the integrator capacitance C1 is then updated. When the gain is decreased by 2 (when Dec becomes high), one half of C1 is disconnected and discharged to ground during φ1 without affecting the output. When it is reconnected to the other half of C1 during φ2, it halves the output voltage. Another capacitor (Cint) of same value as C1 is charged to the output voltage during φ1. When the gain is increased by 2 (when Inc becomes high), Cint is discharged to the input of the OTA during φ2, thereby doubling the output voltage. These compression, expansion and memory update operations are synchronized in discrete time. To reduce complexity, the expansion at the output of each stage is combined with the compression at the input of the following stage resulting in an equivalent gain for the following stage. For each stage, the companding algorithm works on a finite-state machine (FSM) run by a controller consisting of comparators and digital circuits. Since a companding filter is a nonlinear system internally, its performance is affected by any spurious signals arising from within the system. In our case, the OTA's DC offset gives rise to even-order distortion since the DC offset has the same sign in both positive and negative half cycles of the input signal. In a SC ladder type filter, each OTA's output is sampled in both clock phases for both feedforward and feedback paths. Thus, the DC offset of the OTAs should be eliminated in both phases. We use a continuous-time auto-zeroed (AZ) OTA using feedforward [5], which results in a residual offset of 500µV under worst case process and mismatch conditions. Correlated double sampling [5] is also used to make the integration phase offset-free. Using both techniques, a worst case THD of -50dB is achieved from simulations. The AZ OTA consumes 40µW from 1.2V compared to 6mW consumed by the main OTA.

A 34dB SNDR Instantaneously-Companding Baseband SC Filter for 802.11a/g WLAN Receivers

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References:
Figure 4.10.1: Companding SC discrete integrator with timing diagram for the control signals.

Figure 4.10.2: 802.11a WLAN receiver gain distribution for 6 Mb/s rate and 3 input signal levels at -82dBm, -51dBm and -30dBm.

Figure 4.10.3: Signal-to-distortion ratio for single-tone (2MHz) and 2-tone (4.6MHz and 5MHz) tests vs. input signal power in dBm.

Figure 4.10.4: Output frequency spectrum for a 2-tone test (4.6MHz and 5MHz) at an input signal power of -7dBm.

Figure 4.10.5: Single-tone test (2MHz) output voltage waveforms before and after expansion at an input signal power of -4.4dBm.

Figure 4.10.6: Performance summary.
Figure 4.10.7: Die photograph.